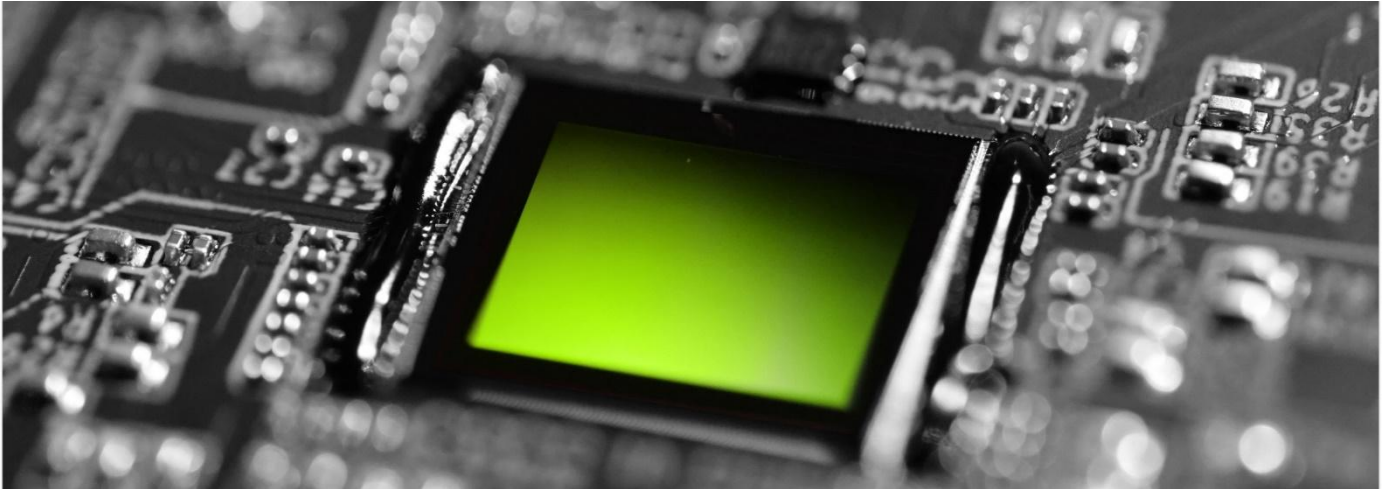
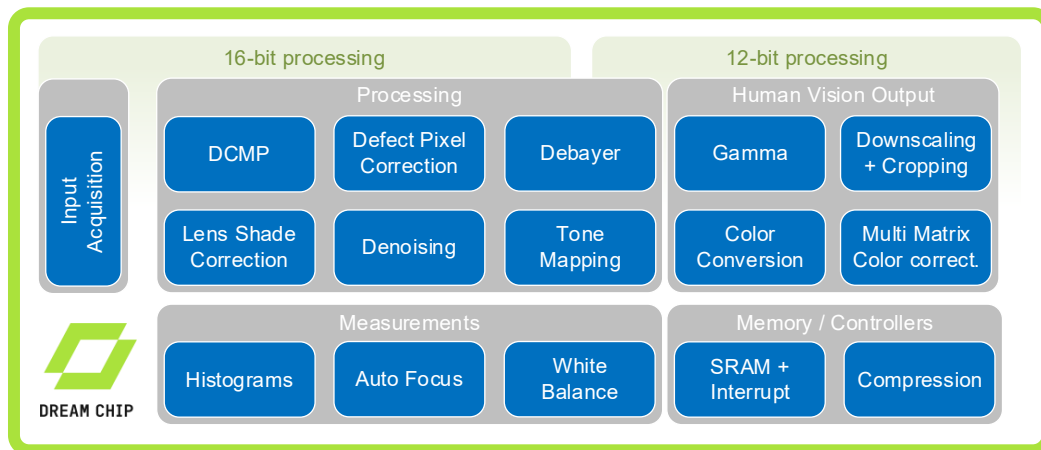




## W Series: *ISP-W114*

Dream Chip's Real-time Pixel Processor for Vision applications is a scalable and configurable Wide Dynamic Range (WDR) capable image signal processor (ISP). The processing pipeline consists of all necessary modules allowing to output WDR tone-mapped images.

The W Series provides configurable input and output data widths. It supports input image frames with 8 to 16-bit amplitude resolutions, while it can output tone-mapped frames with 12 bits per pixel.



The W Series are ISPs which are optimized for area while getting the best image quality. Options to extend pipeline with a Machine Vision output or fusion of multiple input interfaces are possible.

## Specification:

|                     |                                                                                                          |
|---------------------|----------------------------------------------------------------------------------------------------------|
| <b>Sensor input</b> | Bayer / clear pixel / mono<br>RGGB / RCCB / RCCC<br>Configurable 16-bit input – up to 64 Mpix resolution |
| <b>Throughput</b>   | 1.3 gigapixels / second, e.g. 16 MP @ 60 fps                                                             |
| <b>ISP output</b>   | Streaming output for Human Vision (Machine Vision – optional)                                            |

## ISP-Advantages:

- Modular approach
- Scalable resolution up to 64 MP
- Customizations
- Low latency
- Area-optimized
- FPGA validation platforms available
- Tests with different sensors
- Calibration tools
- Bit-true simulation tools
- Software example code

## Applications:

- Surveillance / Security
- High resolution Consumer
- Wearables
- Industrial
- Factory automation
- Robotics
- Image capture
- Digital video recording

[Dream Chip's ISP](#) is designed with a modular approach, allowing seamless scalability to match a wide range of application requirements. This flexibility enables customers to customize functionality, balancing performance, power efficiency, and silicon area optimization. With dynamic resolution from 12 to 28 bits, resolutions up to 64 MP, 120 fps, it delivers **high-speed, high-quality image processing**. Its adaptable architecture allows new features to be integrated or functions to be optimized, ensuring optimal efficiency, reduced power consumption, and a tailored imaging pipeline.

Looking for a **flexible, high-performance ISP solution** tailored to your needs? Let's discuss how [Dream Chip](#) can support your project with **scalable architecture, cutting-edge performance, and expert customization**. **Get in touch with our ISP experts today.**

